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Notice of Allowability	Application No.	Applicant(s)	
	10/053,340	WARE ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	
The MAILING DATE of this communication apperature All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	olication. If not include will be mailed in due	ed course. <b>THIS</b>
1. This communication is responsive to 8/2/03 and 10/24/03.			
2. The allowed claim(s) is/are <u>1-29</u> .			
3. $\boxtimes$ The drawings filed on <u>02 August 2003</u> are accepted by the	Examiner.		
4.			
<ul> <li>Attachment(s)</li> <li>1. ☑ Notice of References Cited (PTO-892)</li> <li>2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)</li> <li>3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 10/24/03</li> <li>4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material</li> </ul>	5. Notice of Informal P 6. Interview Summary Paper No./Mail Dat 7. Examiner's Amendr 8. Examiner's Stateme 9. Other	(PTO-413), te nent/Comment	,

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## **DETAILED ACTION**

1. Claims 1-29 are pending.

2. The preliminary amendment, filed 8/2/03, and IDS, filed 10/24/03, has been considered.

## Allowable Subject Matter

3. Claims 1-29 are allowed.

4. The following is an examiner's statement of reasons for allowance:

5. As to claim 1,5 the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus.

- 6. Claims 2-4,6-8 are also allowable for incorporating the limitations of claim 1/5, and further limitations.
- 7. As to claim 9, the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus and wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus.
- 8. Claims 10-13 are also allowable for incorporating the limitations of claim 9, and further limitations.

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- 9. As to claim 14, the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus uses non-differential signaling.
- 10. Claims 15-17 are also allowable for incorporating the limitations of claim 14, and further limitations.
- 11. As to claim 18, the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus.
- 12. Claims 19-20 are also allowable for incorporating the limitations of claim 18, and further limitations.
- 13. As to claim 21, the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling.

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14. Claims 22-24 are also allowable for incorporating the limitations of claim 21, and further limitations.

- 15. As to claim 25, the prior art of record does not teach nor suggest the claimed memory system. More specifically the prior art does not reasonable suggest a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first memory component includes a first termination structure connected to the first data bus.
- 16. Claims 26-29 are also allowable for incorporating the limitations of claim 25, and further limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 703-305-3866. The examiner can normally be reached on 8am-3pm M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen

Examiner

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